PATENT
790001-2043

AMENDMENT TO THE CLAIMS

Please amend the claims without prejudice, without admission, without surrender of subject matter, and without any intention of creating any estoppel as to equivalents, as follows.

In the Claims:

Claim 1 (Currently amended)

A semiconductor device comprising:

a semiconductor substrate;

a fin-shaped semiconductor layer which is formed on the semiconductor substrate, is long in a first direction and is short in a second direction crossing the first direction;

a gate insulating layer formed on side surfaces of the semiconductor layer in the second direction;

a gate electrode arranged so as to be adjacent to the gate insulating layer;

a channel area formed at a position adjacent to the gate insulating layer in the semiconductor layer;

a source/drain extension area which is formed at a position adjacent to the channel area in the semiconductor layer in the first direction; and

a source/drain area which is formed at a position adjacent to the source/drain extension area in the semiconductor layer in the first direction;

wherein a width of the semiconductor layer in the channel area in the second direction is smaller than a width of the semiconductor layer in the source/drain extension area in the second direction

~~wherein a width of the semiconductor layer in the channel area in the second direction is smaller than a width of the semiconductor layer in the source/drain area in the second direction~~.

Claim 2 (Currently amended)

The semiconductor device according to claim 1, wherein the width of the semiconductor layer in the channel area in the second direction is smaller than a width of the semiconductor layer in the source/drain area in the second direction ~~wherein the width of the semiconductor layer in the channel area in the second direction is smaller than a width of the semiconductor layer in the source/drain extension area in the second direction~~.

Claim 3 (Original)
The semiconductor device according to claim 2, wherein the width of the semiconductor layer in the source/drain extension area in the second direction is smaller than the width of the semiconductor layer in the source/drain area in the second direction.

Claim 4 (Original)
The semiconductor device according to claim 2, wherein the width of the semiconductor layer in the source/drain extension area in the second direction is equal to the width of the semiconductor layer in the source/drain area in the second direction.

Claim 5 (Original)
The semiconductor device according to claim 1, wherein the width of the semiconductor layer in the channel area in the second direction is smaller than a gate length of the gate electrode.

Claim 6 (Original)
The semiconductor device according to claim 1, wherein the width of the semiconductor layer in the source/drain extension area in the second direction is equal to or larger than a gate length of the gate electrode.

Claim 7 (Original)
The semiconductor device according to claim 1, wherein the gate electrode is constituted by a first part which is formed on one side of the semiconductor layer in the second direction and a second part which is formed on the other side of the semiconductor layer in the second direction.

Claim 8 (Currently amended)
A semiconductor device comprising:

a semiconductor substrate;

a plurality of fin-shaped first semiconductor layers which are formed on the semiconductor substrate, long in a first direction, short in a second direction crossing the first direction, and aligned in the second direction;

a second semiconductor layer which connects a plurality of the first semiconductor layers with each other at end portions of a plurality of the first semiconductor layers in the first direction;

a gate insulating layer which is formed on side surfaces of each of a plurality of the first semiconductor layers in the second direction;

a gate electrode arranged so as to be adjacent to the gate insulating layer;

a channel area which is formed at a position adjacent to the gate insulating layer in a plurality of the first semiconductor layers;

a source/drain extension area formed at a position adjacent to the channel area in the first direction in a plurality of the first semiconductor layers; and

a source/drain area formed at a position adjacent to the source/drain extension area in the second semiconductor layer in the first direction[[.]];

wherein a width of each of a plurality of the first semiconductor layers in the channel area in the second direction is smaller than a width of each of a plurality of the first semiconductor layers in the source/drain extension area in the second direction.

Claim 9 (Original)
The semiconductor device according to claim 8, wherein heights of a plurality of the first semiconductor layers are all equal to each other.

Claim 10 (Original)
The semiconductor device according to claim 8, wherein the inside of the second semiconductor layer all consists of the source/drain area.

Claim 11 (Cancelled)

Claim 12 (Original)
The semiconductor device according to claim 8, wherein the width of the first semiconductor layer in the source/drain extension area in the second direction is smaller than a width of the second semiconductor layer in the source/drain area in the second direction.

Claim 13 (Original)

The semiconductor device according to claim 8, wherein the width of the first semiconductor layer in the channel area in the second direction is smaller than a gate length of the gate electrode.

Claim 14 (Currently amended)

A semiconductor device comprising:

a semiconductor substrate;

a fin-shaped semiconductor layer which is formed on the semiconductor substrate, is long in a first direction and is short in a second direction crossing the first direction;

a gate insulating layer formed on side surfaces of the semiconductor layer in the second direction;

a gate electrode arranged so as to be adjacent to the gate insulating layer;

a channel area formed at a position adjacent to the gate insulating layer in the semiconductor layer;

a source/drain extension area formed at a position adjacent to the channel area in the semiconductor layer in the first direction;

a source/drain area formed at a position adjacent to the source/drain extension area in the semiconductor layer in the first direction; and

a silicide layer which is formed on a surface portion of the semiconductor layer in the source/drain layer but not formed in the inner portion of the same[[.]];

wherein a width of each of a plurality of the first semiconductor layers in the channel area in the second direction is smaller than a width of each of a plurality of the first semiconductor layers in the source/drain extension area in the second direction.

Claim 15 (Original)

The semiconductor device according to claim 14, wherein the silicide layer is formed on an upper portion of the semiconductor layer and a surface portion of the same in the second direction.

Claim 16 (Original)
The semiconductor device according to claim 15, wherein an insulating layer which functions as a stopper in silicidation is formed between the silicide layer on the upper portion of the semiconductor layer and the semiconductor layer.

Claim 17 (Original)
The semiconductor device according to claim 14, wherein a width of the semiconductor layer in the second direction is double-larger than a width of the silicide layer in the second direction which is formed on the surface portion of the semiconductor layer in the second direction.

Claim 18 (Original)
The semiconductor device according to claim 14, wherein a width of the semiconductor layer in the source/drain area in the second direction is larger than a width of the semiconductor layer in the source/drain extension area or the channel area in the second direction.

Claim 19 (Original)
The semiconductor device according to claim 14, wherein a height of the semiconductor layer in the source/drain area is larger than a height of the semiconductor layer in the source/drain extension area or the channel area.

Claims 20-27 (Cancelled)